CLAIMS

We claim:

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1	1). A method, comprising:
2	determining when an operation on a larger data type may be replaced by
3	the operation on a smaller data type having a reduced precision,
4	wherein the operation is contained in code associated with a language
5	implementation system; and
6	replacing the operation on the larger data type by the operation on the
7	smaller data type.
1	2). The method of claim 1, further comprising:
2	determining when a first variable of the larger data type may be replaced
3	by a second variable of a smaller data type having the reduced
4	precision; and
5	replacing the first variable of the larger data type by the second variable o
6	the smaller data type.
1	3). The method of claim 2, wherein replacing the operation and replacing the firs
2	variable are used for automatic vectorization for signal and media processors
3	that provide vector operations on small fixed-point data types.

- 1 4). The method of claim 3, wherein the processors are MMX equipped.
- 5). The method of claim 3, wherein the processors are SSE equipped.
- 1 6). The method of claim 3, further comprising performing algebraic simplification on the code.

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MMX equipped.

1	7). The method of claim 6, wherein the language implementation system		
2	performs bitwise constant propagation by abstract interpretation on the code.		
1	a) A computer readable medium having stored thereon a plurality of		
1	8). A computer-readable medium having stored thereon a plurality of		
2	instructions, said plurality of instructions when executed by a computer,		
3	cause said computer to perform:		
4	determining when an operation on a larger data type may be replaced by		
5	the operation on a smaller data type having a reduced precision,		
6	wherein the operation is contained in code associated with a language		
7	implementation system; and		
8	replacing the operation on the larger data type by the operation on the		
9	smaller data type.		
1	9). The computer-readable medium of claim 8 having stored thereon additional		
2	instructions, said additional instructions when executed by a computer for		
3	optimizing, cause said computer to further perform:		
4	determining when a first variable of the larger data type may be replaced		
5	by a second variable of a smaller data type having the reduced		
6	precision; and		
7	replacing the first variable of the larger data type by the second variable of		
8	the smaller data type		
1	10). The computer-readable medium of claim 9 wherein replacing the		
2	operation and replacing the first variable are used for automatic vectorization for		
3	signal and media processors that provide vector operations on small fixed-point		
4	data types.		
4	data typool		

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The computer-readable medium of claim 10, wherein the processors are

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1	12).	The computer-readable medium of claim 10, wherein the processors are	
2	SSE equipped.		
1	13).	The computer-readable medium of claim 10, having stored thereon	
2	additional instructions, said additional instructions when executed by a		
3	computer for optimizing, cause said computer to further perform performing		
4	algebraic simplification on the code.		
1	14).	The computer-readable medium of claim 13, wherein the language	
2	implementation system performs bitwise constant propagation by abstract		
3	int	terpretation on the code.	
1	15\	A avotom, comprising:	
1	15).	A system, comprising:	
2	'	processor;	
3	m	emory connected to the processor storing instructions for type demotion of	
4		expressions and variables by bitwise constant propagation executed by	
5		the processor;	
6	st	orage connected to the processor that stores a software code having a	
7		plurality of separately compilable routines,	
8	W	herein the processor executes the instructions on the code to	
9		determine when an operation on a larger data type may be replaced by	
10		the operation on a smaller data type having a reduced precision,	
11		wherein the operation is contained in code associated with a language	
12		implementation system; and	

replace the operation on the larger data type by the operation on the

smaller data type.

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- 1 16). The system of claim 15, wherein the processor further determines when a
 2 first variable of the larger data type may be replaced by a second variable
 3 of a smaller data type having the reduced precision; and
 4 replaces the first variable of the larger data type by the second variable of
 5 the smaller data type.
- 1 17). The system of claim 16, wherein the processor replaces the operation and replaces the first variable to provide vector operations on small fixed-point data types.
- 1 18). The system of claim 17, wherein the processor is MMX equipped.
- 1 19). The system of claim 17, wherein the processor is SSE equipped.
- 1 20). The system of claim 18, wherein the processor performs algebraic simplification on the code.
- 1 21). The system of claim 19, wherein the language implementation system performs bitwise constant propagation by abstract interpretation on the code.
- 1 22). A system, comprising:
- means for determining when an operation on a larger data type may be
- 3 replaced by the operation on a smaller data type having a reduced
- 4 precision, wherein the operation is contained in code associated with a
- 5 language implementation system; and
- 6 means for replacing the operation on the larger data type by the operation
- 7 on the smaller data type.
- 1 23). The system of claim 22, further comprising:

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2	means for determining when a first variable of the larger data type may be
3	replaced by a second variable of a smaller data type having the reduced
4	precision; and
5	means for replacing the first variable of the larger data type by the second
6	variable of the smaller data type.

- 24). The system of claim 23, wherein the means for replacing the operation
 and the means for replacing the first variable are used for automatic
 vectorization for signal and media processors that provide vector operations
 on small fixed-point data types.
- 1 25). The system of claim 24, wherein the processors are MMX equipped.
- 1 26). The system of claim 24, wherein the processors are SSE equipped.
- 27). The system of claim 24, further comprising means for performing
 algebraic simplification on the code.
- 1 28). The system of claim 27, wherein the language implementation system performs bitwise constant propagation by abstract interpretation on the code.

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